A NEW DIRECT MILLIMETER WAVE SIX-PORT RECEIVER

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***Abstract* - A new direct conversion wide band (23 GHz – 31 GHz) six-port millimeter wave receiver suitable for integrated circuit fabrication is proposed to satisfy mass-market wireless communications. The receiver contains one multi chip module (MCM) consisting of a wide band six-port junction, four RF detectors (Schottky diodes), video amplifiers and I&Q decoder. The prototype circuits are fabricated in hybrid integrated circuits, and the receiver topology is suitable for fabrication in microwave monolithic integrated circuits (MMICs). This new hardware receiver is proposed as a robust, rugged, low cost receiver for use in wide band wireless mass market QPSK communications. Hand held and laptop terminals for future e-mail/multi-media services are a prime example of communication equipment needing such receivers. BER measurements and simulation results are presented in the presence of noise, adjacent signal interference, local oscillator (LO) phase shift and LO phase noise.**

I. INTRODUCTION

It is widely recognized that direct conversion receivers offer unique advantages in wireless communications by reducing circuit complexity and allowing a higher level of circuit integration than traditional heterodyne receivers [1]. Six-port direct conversion receivers have been proposed [2]-[5] as multi-mode or software receivers operated with DSPs programmed for a number of modulation schemes.

This paper presents recent results obtained on a new six-port based hardware type receiver designed with application specific circuits (ASC) for QPSK communications. The proposed millimeter wave ASC approach is useful to design other hardware receivers at lower or higher operating frequencies (microwaves and sub-millimeter waves) using either discrete [3], [5] or distributed parameter [2], [4] six-ports. This six-port receiver is designed to operate without the need for precise power readings nor the use of digital signal processor (DSP) as required in previous six-port receivers.

The proposed receiver architecture is chosen to satisfy requirements of hardware receivers used in high speed QPSK communications. The maximum bit rate is solely limited by speed of video and decoder circuits such that data rates of several hundred Mbps can be achieved at low cost. RF and demodulation test results in the presence of noise, adjacent channel interference, local oscillator phase shift and phase noise are presented at data rates of 40 Mbps.

II. RECEIVER ARCHITECTURE AND OPERATING PRINCIPLE

Fig. 1 shows hardware receiver architecture with a number of circuit functions to provide I&Q data directly from received QPSK signals.

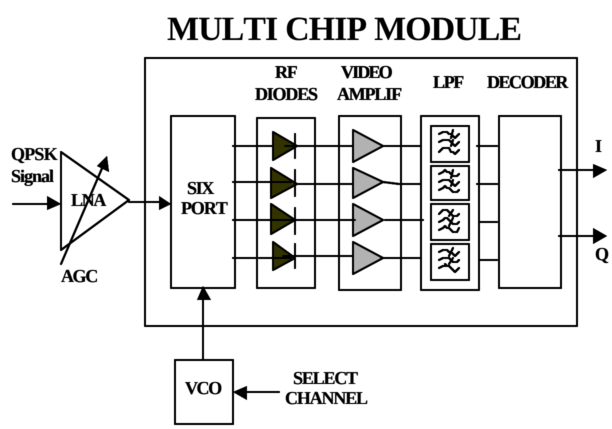

Fig. 1. Receiver architecture

Fig. 2 gives RF topology of wide band millimeter wave distributed parameter six-port junction with RF diodes and matching circuits. Fig. 3 shows circuits used for video amplifiers, integrated active low pass filter (LPF) and analogue decoder circuit. The active low pass filter has a cut-off frequency of 100 MHz corresponding to maximum base band requirement for QPSK test signals used. The RF design of six-port junction is such that only one of four possible modulation states is correctly identified, at any one time, by analogue decoder. The wave shapes of Fig. 4

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show that each output voltage of Fig. 2 has a single minimum value during 360° phase-shift between RF input and VCO signals.

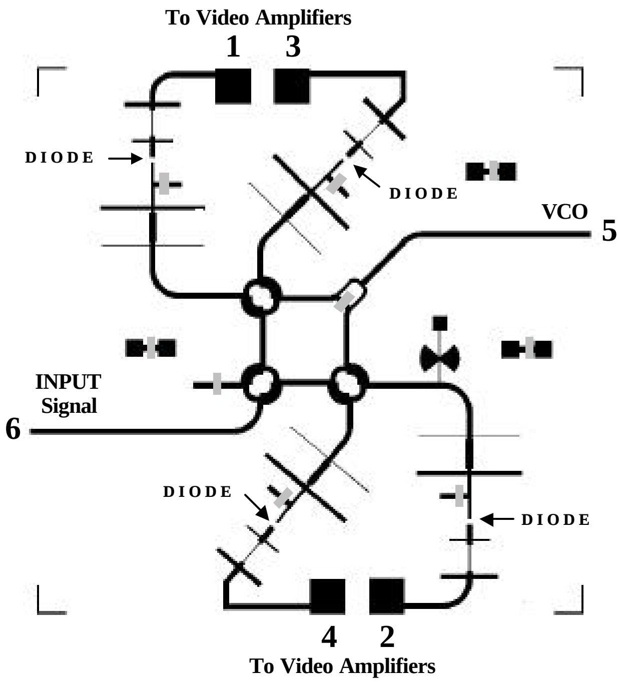

Fig. 2. Six-port junction and matching detector RF circuits

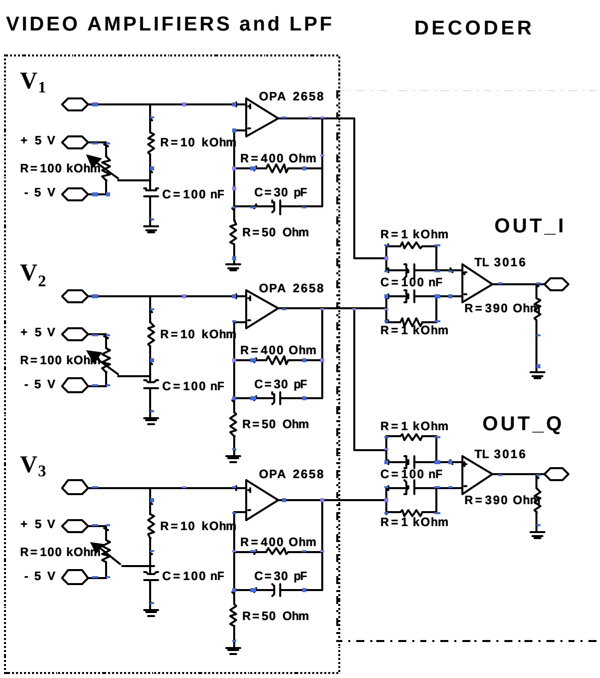

Fig. 3. Active integrated LPFs , video amplifiers and analog decoder circuit

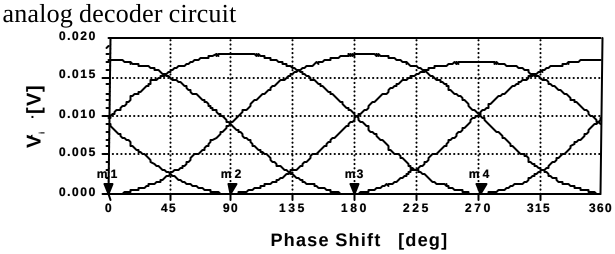

Fig. 4. The detector's output voltages to input signal/VCO phase shift

Input and output simulated I&Q wave shapes given in Fig.5 confirm operating principle of receiver.

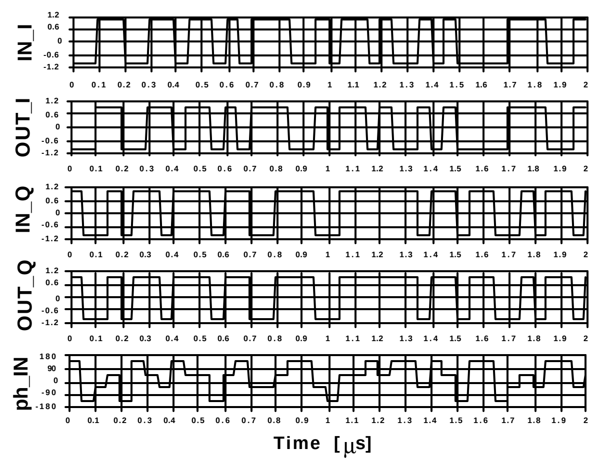

Fig. 5. Receiver **s**imulation results of input and output I&Q wave shapes as function of time

III. Prototype And Test Results

Fig. 6 shows photograph of MCM including ASCs of Fig. 2 and 3 with six-port fabricated in Miniature Hybrid Microwave Integrated Circuit (MHMIC) technology. It is to be noted that a front-end of this receiver can be designed to integrate a number of RF components (VCO, LNA, six-port junction and RF diodes with matching circuits) in MMIC technology. Fig. 7 shows simulated and measured BER as function of E_b/N_O ratio, where E_b is the average energy of a modulated bit and N_O is the noise power spectral density. It is seen that at frequencies within operating band (23 GHz – 31 GHz), the BER is less than 1.0E-6 for E_b/N_O greater then 10 dB. Outside the upper and lower limits of operating bandwidth the BER rises rapidly:

it was measured to be greater than 1.0E-4 at 22 GHz and 32 GHz for the same value of E_b/N_O. Fig. 8 shows results of measured and simulated BER vs. RF signal power level at LNA port of MCM (Fig. 6) with local oscillator signal power of –20 dBm. From results in Fig. 8, it is seen that a minimum signal level of -36 dBm is satisfactory to operate the MCM. The maximum power level of RF input signal was measured to be 3 dBm before BER rapidly deteriorated. Hence, dynamic range of MCM alone is about 40 dB when local oscillator power level is set at -20 dBm. The dynamic range of receiver can be increased well above 70 dB with AGC in LNA. Fig. 9 shows simulated and measured results on BER vs. phase difference (shift) between carrier and local oscillator signals when both frequencies are set at 27 GHz. Fig. 10 shows simulated BER vs. E_b/N_O for different LO phase noise levels. Fig. 11 shows measured BER for amplitude and frequency variations of a CW interference signal using QPSK signals received at rate of 40 Mbps. It is seen that BER is less than 1.0E-6 when Δfr frequency for interference signal is more than twice the cut-off frequency of low pass filter (200 MHz) and its power level is 3 dB above carrier level (–20 dBm). Fig. 12 shows that the maximum bit rate for MCM of Fig. 6 is 58 Mbps.

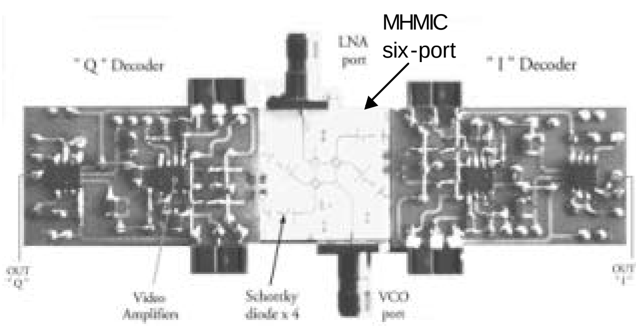

Fig. 6. Photograph of MCM (100mm x 25 mm) given in block diagram of Fig.1

Table 1 shows simulated and measured S parameters of six-port junction with an isolation of at least 27 dB (S56) between LNA port and VCO port of MCM.

IV. CONCLUSIONS

A new direct conversion hardware receiver based on six-port technology suitable for mass-market wide band millimeter wave applications is presented. The proposed concept was verified by measurements and simulations made on hybrid integrated circuit prototype having an operating band of 8 GHz (23 GHz - 31 GHz). BER results on operating dynamic range, signal to noise ratio, signal interference and VCO phase noise measurement encourage fabrication of MMIC integrated front ends of this receiver.

ACKNOWLEDGEMENTS

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TABLE I
SCATTERING PARAMETERS OF SIX-PORT JUNCTION AT 27 GHz

S Parameters	Simulations [dB]	Measurements [dB]
S11	- 38.9	- 27.0
S22	- 31.2	- 25.0
S33	- 28.8	- 24.0
S44	- 30.9	- 25.0
S55	- 38.0	- 27.0
S66	- 30.4	- 25.0
S56	- 33.5	- 27.0

S51	- 6.3	- 6.4
S52	- 6.4	- 6.5
S53	- 6.4	- 6.5
S54	- 6.2	- 6.4
S61	- 6.2	- 6.5
S62	- 6.3	- 6.5
S63	- 6.1	- 6.4
S64	- 6.5	- 6.6

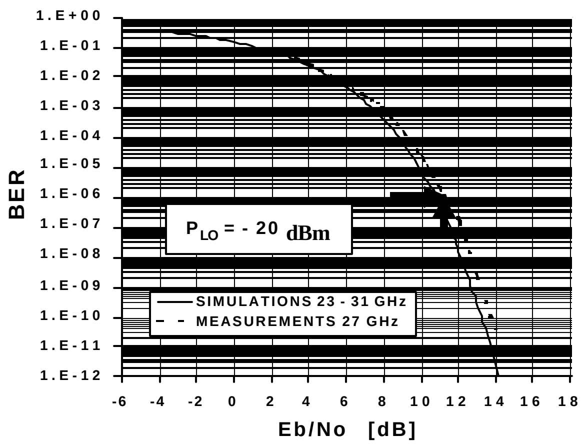

Fig.7. Measured and simulated BER vs. E_b/N_o over operating band (23 GHz – 31 GHz)

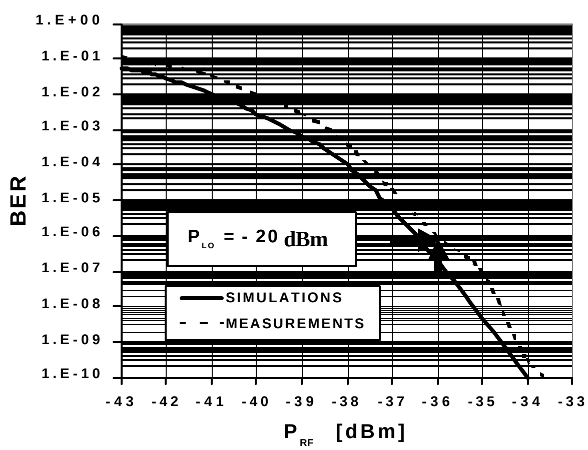

Fig.8. Measured and simulated BER vs. RF power level at LNA port of Fig.5 for carrier frequency of 27 GHz

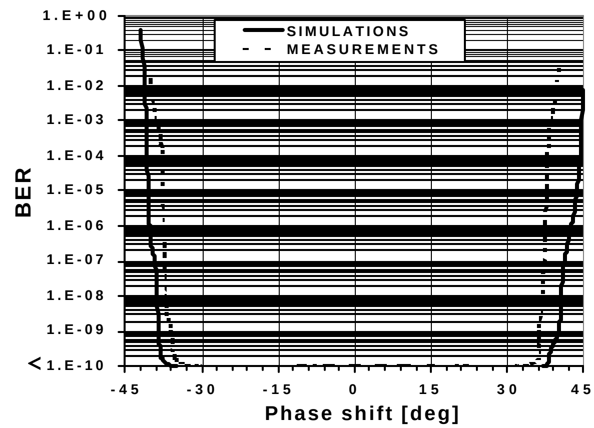

Fig.9. Measured and simulated BER vs. local oscillator phase shift from synchronism (0 deg)

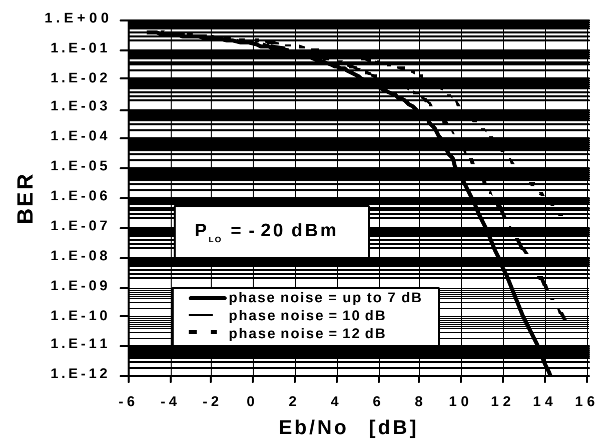

Fig.10. Simulated BER vs. E_b/N_0 for different LO phase noise levels

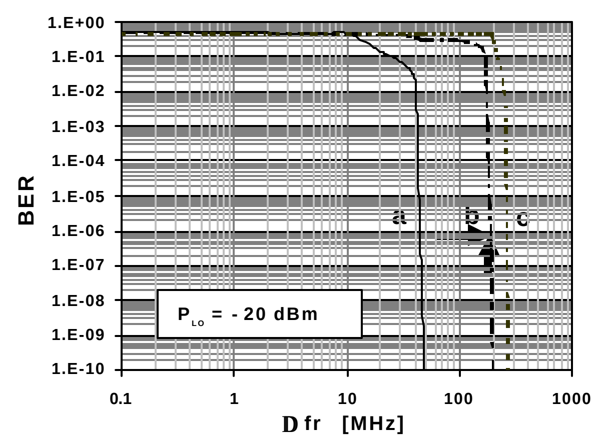

Fig.11. Measured BER vs. frequency difference (Δfr) between carrier (27 GHz) and CW interference signal. Data

rate is 40 Mbps and interference signal power levels above carrier (- 20 dBm): a) 0 dB, b) 3 dB, c) 6 dB

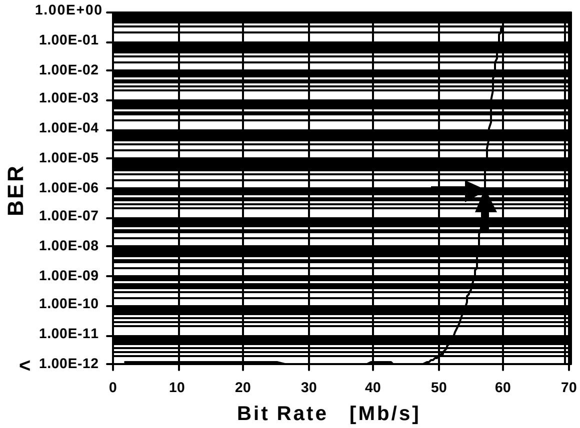

Fig.12. Measured BER vs. bit rate